What is claimed is:

1. A switching arrangement comprising:

a digital input comprising a first digital input portion and a second digital input portion;

a digital output comprising a first digital output portion and second digital output portion;

a switching element between the digital input and the digital output, the switching element having a first condition allowing the first digital output portion to correspond to the first digital input portion and the second digital output portion to correspond to the second digital input portion, and a second condition allowing the first digital output portion to correspond to the second digital input portion and the second digital output portion to correspond to the first digital input portion; and

a control arrangement to switch the switching element between the first condition and the second condition.

2. The switching arrangement of claim 1, wherein the control arrangement comprises analog processing elements.

3. The switching arrangement of claim 1, wherein the control arrangement has a first control input connected with the first digital input portion, a second control input connected with the second digital input portion, and a control output, the control output allowing the switching element to assume the second condition if the first digital input portion is different from the second digital input portion.

4. The switching arrangement of claim 3, wherein the control arrangement comprises a subtractor, subtracting the first digital input portion from the second digital input portion, the subtractor having a subtractor output with a first subtractor output value if the first digital input portion is not in a predetermined relationship with the second digital input portion and a second subtractor output

value if the first digital input portion is in a predetermined relationship with the second digital input portion.

5. The switching arrangement of claim 4, wherein the predetermined relationship between the first digital input portion and the second digital input portion is that the first digital input portion is identical to the second digital input portion.

6. The switching arrangement of claim 4, wherein the first digital input portion and the second digital input portion are multi-bit inputs comprising high digital values and low digital values, and wherein the predetermined relationship between the first digital input portion and the second digital input portion is that a sum between the high digital values of the first digital input portion is identical to a sum between the high digital values of the second digital input portion.

7. The switching arrangement of claim 4, wherein the control arrangement comprises a delta-sigma modulator, the subtractor output being input into the delta-sigma modulator.

8. The switching arrangement of claim 7, wherein the delta-sigma modulator comprises a quantizer having a quantizer input and a quantizer output.

9. The switching arrangement of claim 8, wherein the delta-sigma modulator comprises:

a filtering element, having a filter element input and a filter element output, the filtering element output corresponding to the quantizer input; and

a digital-to-analog converter (DAC) having a DAC input and a DAC output, the DAC output corresponding to the resonator input.

10. The switching arrangement of claim 9, wherein the filtering element is a second-order resonator.

11. The switching arrangement of claim 9, wherein the filtering element is an integrator.

12. The switching arrangement of claim 9, wherein the filtering element is a differentiator.

13. The switching arrangement of claim 9, wherein the control arrangement further comprises a multiplier, the multiplier multiplying the subtractor output with the quantizer output.

14. The switching arrangement of claim 13, wherein a signal fed between the multiplier and the DAC input is a ternary signal.

15. The switching arrangement of claim 14, wherein the ternary signal has –1, 0, + 1 values.

16. The switching arrangement of claim 9, wherein the subtractor is a XOR gate.

17. The switching arrangement of claim 16, wherein the control arrangement further comprises a multiplexer, the multiplexer selecting among the quantizer output and an auxiliary value based upon the value of the subtractor output.

18. The switching arrangement of claim 1, wherein the switching element is a multiplexer.

19. The switching arrangement of claim 18, wherein the switching element is a latched multiplexer.

20. The switching arrangement of claim 9, wherein the DAC comprises:
a first analog DAC transconductor having a variable gain; and
a second analog DAC transconductor.

21. The switching arrangement of claim 10, wherein the resonator comprises:

a first analog resonator transconductor having a variable gain;

a second analog resonator transconductor;

a first delay element; and

a second delay element..

22. The switching arrangement of claim 16, wherein the DAC comprises a first analog DAC transconductor having a variable gain and a second analog DAC transconductor, the resonator comprising:

a first analog resonator transconductor having a variable gain;

a second analog resonator transconductor;

a first delay element having a first delay element input;

a second delay element having a second delay element input;

a first adder, adding the output of the first delay element with the output of the first analog DAC transconductor and the output of the first analog resonator transconductor; and

a second adder, adding the output of the second analog DAC transconductor with the output of the second analog resonator transconductor.

23. The switching arrangement of claim 22, wherein the output of the first delay element is fed back to the input of the first analog resonator transconductor, to the input of the second analog resonator transconductor, and to the input of the quantizer.

24. The switching arrangement of claim 22, wherein the subtractor output is input into the sigma-delta modulator by means of a multiplexer located between the quantizer output and the DAC input, and wherein the multiplexer is incorporated into the first analog DAC transconductor and the second analog DAC transconductor.

25. The switching arrangement of claim 23, wherein the subtractor output is input into the sigma-delta modulator by means of a multiplexer located between the quantizer output and the DAC input, and wherein the multiplexer is

incorporated into the first analog DAC transconductor and the second analog DAC transconductor.

26. The switching arrangement of claim 20, wherein the first analog DAC transconductor is frequency controlled.

27. The switching arrangement of claim 22, wherein the first analog resonator transconductor is frequency controlled.

28. The switching arrangement of claim 21, wherein the first delay element has a controllable gain.

29. The switching arrangement of claim 28, wherein the first delay element comprises a first switched emitter follower track-and-hold amplifier, a second switched emitter follower track-and-hold amplifier, and an adjustable gain amplifier between the first switched emitter follower track-and-hold amplifier and the second switched emitter follower track-and-hold amplifier.

30. The switching arrangement of claim 22, wherein the resonator comprises a third analog resonator transconductor.

31. The switching arrangement of claim 30, further comprising a first resistor placed before the first delay element input and a second resistor placed before the second delay element input.

32. The switching arrangement of claim 8, wherein the quantizer comprises three latch elements.

33. The switching arrangement of claim 4, wherein the subtractor is an XOR gate and the first and second digital input are thermometer coded.

34. A circuit comprising:
a first input and a second input;

a control element connected with the first input and second input;

a switch either switching or not switching the first input and the second input according to the control element; and

a clocking arrangement to pipeline the switch.

35. The circuit of claim 34, wherein the first input and the second input are digital inputs.

36. The circuit of claim 34, wherein the control element comprises a delta-sigma modulator.

37. The circuit of claim 34, wherein the delta-sigma modulator comprises a filtering element and a quantizer, and wherein the clocking arrangement clocks the filtering element and the quantizer.

38. The circuit of claim 37, wherein the filtering element comprises at least one delay element, the at least one delay element clocked by the clocking arrangement.

39. The circuit of claim 38, wherein the clocked delay element comprises a first switched emitter follower track-and-hold amplifier, a second switched emitter follower track-and-hold amplifier, and an adjustable gain amplifier between the first switched emitter follower track-and-hold amplifier and the second switched emitter follower track-and-hold amplifier.

40. The circuit of claim 37, wherein the quantizer comprises a plurality of latches.

41. A circuit comprising:

a first input and a second input;

a control element connected with the first input and the second input;

a switch either switching or not switching the first input and the second input according to the control element; and

a tuning arrangement to frequency-adjust the switch.

42. The circuit of claim 41, wherein the first input and the second input are digital inputs.

43. The circuit of claim 41, wherein the control element comprises a delta-sigma modulator.

44. The circuit of claim 43, wherein the delta-sigma modulator comprises a filtering element and a quantizer.

45. The circuit of claim 44, wherein the filtering element comprises at least one delay element.

46. The circuit of claim 45, wherein the delay element comprises an adjustable gain circuit.

47. The circuit of claim 44, wherein the filtering element further comprises a plurality of transconductors, and wherein the tuning arrangement frequency-adjusts at least one transconductor of the plurality of transconductors.

48. A switching arrangement comprising:

a first digital input;

a second digital input;

a switch for switching the first digital input and the second digital input;

an evaluation element connected with the first digital input and the second digital input, the evaluation element evaluating whether the first digital input and the second digital input are in a predetermined relationship therebetween;

a control element to control switching of the switch, the control element connected with the evaluation element and the switching element, the control element comprising a quantizer having a quantizer output, wherein switching between the first digital input and the second digital input depends on the

quantizer output when the first digital input and the second digital input are in the predetermined relationship therebetween and switching between the first digital input and the second digital input does not depend on the quantizer output when the first digital input and the second digital input are not in the predetermined relationship therebetween.

49. The switching arrangement of claim 48, wherein the predetermined relationship between the first digital input and the second digital input is that the first digital input is identical to the second digital input.

50. The switching arrangement of claim 48, wherein the first digital input and the second digital input are multi-bit inputs comprising high digital values and low digital values, and wherein the predetermined relationship between the first digital input and the second digital input is that a sum between the high digital values of the first digital input is identical to a sum between the high digital values of the second digital input.

51. The switching arrangement of claim 48, wherein the quantizer is part of a delta-sigma modulator.

52. The switching arrangement of claim 51, wherein the delta-sigma modulator further comprises a filtering element and a digital-to-analog converter (DAC).

53. A mismatch error shaper comprising:

a) a digital input comprising a plurality of bits;

b) a plurality of routing blocks routing the bits of the plurality of bits, wherein each routing block of the plurality of routing blocks comprises:

b1) a digital input having a first digital input portion and a second digital input portion;

b2) a switch for switching the first digital input portion and the second digital input portion;

b3) an evaluation element connected with the first digital input portion and the second digital input portion, the evaluation element evaluating whether the first digital input portion and the second digital input portion are in a predetermined relationship therebetween;

b4) a control element to control switching of the switch, the control element comprising a quantizer having a quantizer output, wherein switching between the first digital input portion and the second digital input portion depends on the quantizer output when the first digital input portion and the second digital input portion are in the predetermined relationship therebetween and switching between the first digital input portion and the second digital input portion does not depend on the quantizer output when the first digital input portion and the second digital input portion are not in the predetermined relationship therebetween;

c) a plurality of digital outputs; and

d) an adder, adding the outputs of the plurality of digital outputs.

54. The mismatch error shaper of claim 53, further comprising a clock arrangement to pipeline the routing blocks.

55. The mismatch error shaper of claim 53, further comprising a tuning arrangement connected with the routing blocks, to shape errors away from a desired frequency band.

56. The mismatch error shaper of claim 53, wherein the quantizer is part of a delta-sigma modulator.

57. The mismatch error shaper of claim 56, wherein the delta-sigma modulator further comprises a filtering element connected with the quantizer.

58. The mismatch error shaper of claim 57, wherein the filtering element is selected from the group consisting from a resonator, an integrator, and a differentiator.

59. The mismatch error shaper of claim 57, wherein the filtering element is a second-order resonator.

60. The mismatch error shaper of claim 59, wherein the second-order resonator comprises:

a first analog resonator transconductor;

a second analog resonator transconductor;

a first delay element;

a second delay element; and

an adder adding the output of the first delay element with the output of the first analog resonator transconductor.

61. The mismatch error shaper of claim 60, wherein the first analog resonator transconductor has a variable gain.

62. The mismatch error shaper of claim 57, further comprising a digital-to-analog converter (DAC) connected with the filtering element.

63. The mismatch error shaper of claim 62, wherein the DAC is frequency controlled.

64. The mismatch error shaper of claim 62, wherein the DAC comprises:

a first analog DAC transconductor; and

a second analog DAC transconductor.

65. The mismatch error shaper of claim 64, wherein the first analog DAC transconductor has a variable gain.

66. The mismatch error shaper of claim 65, wherein the first analog DAC transconductor is frequency controlled.

67. The mismatch error shaper of claim 60, wherein the first analog resonator transconductor is frequency controlled.

68. A method comprising:

providing a digital input comprising a first digital input portion and a second digital input portion;

providing a digital output comprising a first digital output portion and a second digital output portion; and

either switching the first digital input portion and the second digital input portion, to make the first digital input portion correspond with the second digital output portion and the second digital input portion correspond with the first digital output portion, or not switching the first digital input portion and the second digital input portion, to make the first digital input portion correspond with the first digital output portion and the second digital input portion correspond with the second digital output portion,

wherein switching is performed when the first digital input portion and the second digital input portion are in a predetermined relationship therebetween, and not switching is performed when the first digital input portion and the second digital input portion are not in the predetermined relationship therebetween.

69. A method for testing mismatch shaping comprising:

providing a circuit, the circuit comprising a first input and a second input, a control arrangement; and a switching arrangement either switching or not switching the first input and the second input according to the control arrangement, the circuit having a first circuit output and a second circuit output;

providing a first DAC having a first DAC input and a second DAC input;

providing a second DAC having a second DAC input and a second DAC output;

connecting the first circuit output with the first DAC input and the second circuit output with the second DAC input;

subtracting the second DAC output from the first DAC output to provide a difference output; and

inputting the difference output to a spectrum analyzer.